Document Title

256K x 8 Hight Speed SRAM with 3.3V

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	September 12,2001	

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256K x 8 HIGH-SPEED CMOS STATIC RAM

FEATURES

- High-speed access times:
  — 8, 10, 12 and 15 ns
- High-preformance, lower-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- CMOS power: 540 mW @ 10 ns
  36 mW standby mode
- TTL compatible inputs and outputs
- Single 3.3V ± 10% power supply
- Packages available:
  — 36-pin 400mil SOJ
  — 44-pin TSOP-2

DESCRIPTION

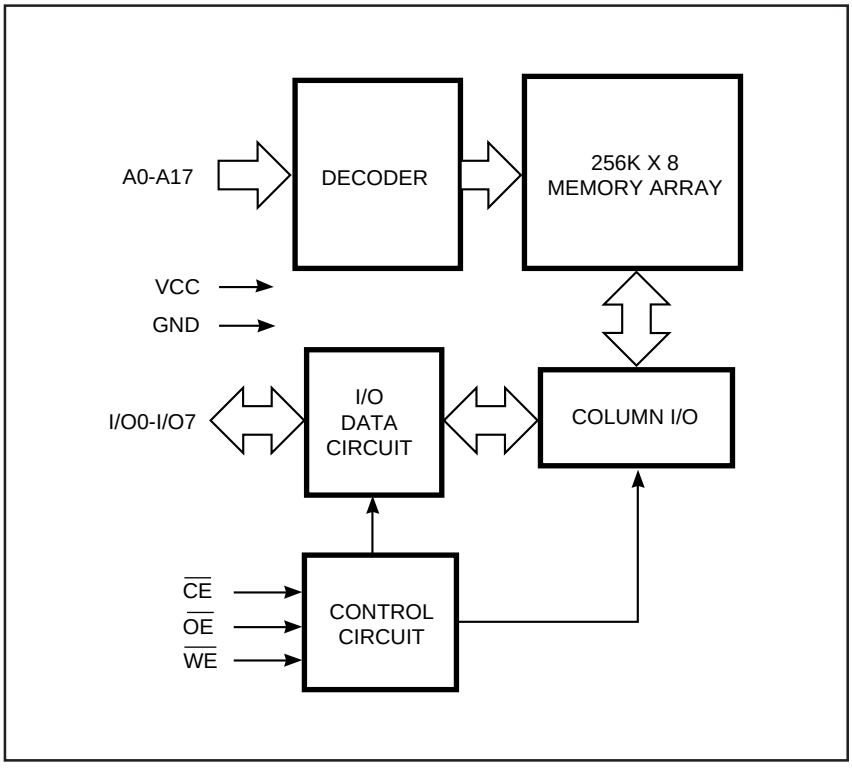
The *ICSI* IC61LV2568 is a very high-speed, low power, 262,144-word by 8-bit COMS static RAM. The IC61LV2568 is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher preformance and low power consumotion devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 36 mW (max.) with CMOS input levels.

The IC61LV2568 operates from a single 3.3V power supply and all inputs are TTL-compatible.

The IC61LV2568 is available in 36-pin, 400mil SOJ and 44-pin TSOP-2 package.

FUNCTIONAL BLOCK DIAGRAM



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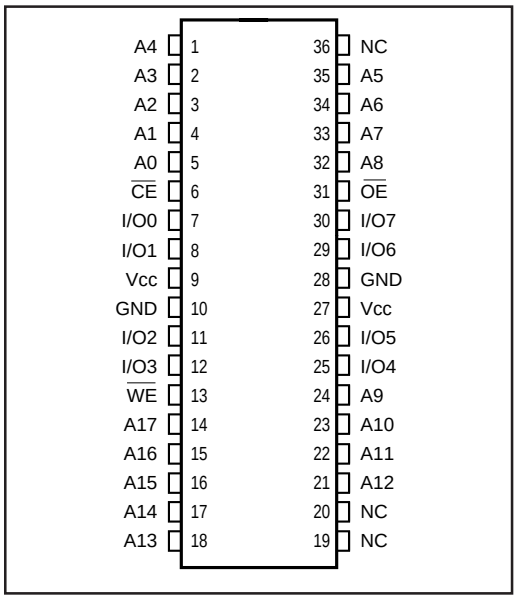
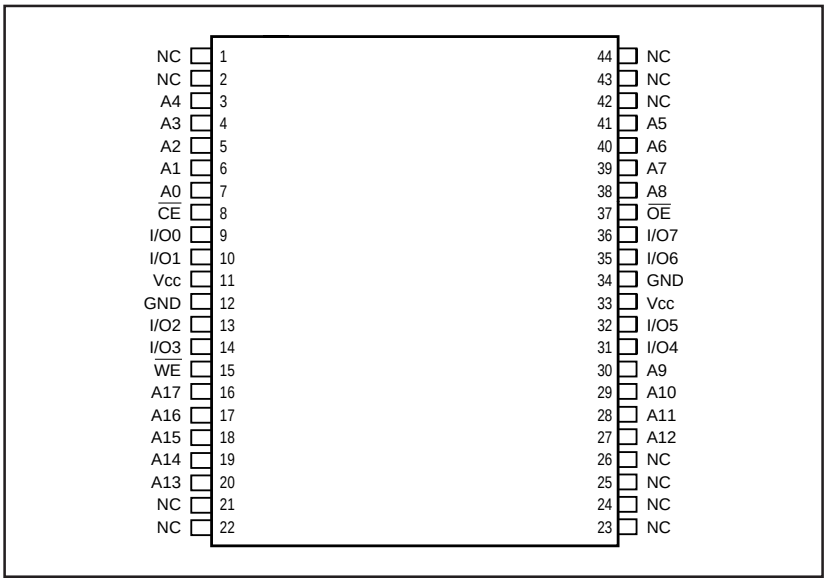
PIN CONFIGURATION
36-Pin SOJ



PIN CONFIGURATION
44-Pin TSOP-2



PIN DESCRIPTIONS

A0-A17	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply Voltage Relative to GND		–0.5 to +4.6	V
V_{TERM}	Terminal Voltage with Respect to GND		–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	Com.	–10 to +85	°C
		Ind.	–45 to +90	
T_{STG}	Storage Temperature		–65 to +150	°C
P_D	Power Dissipation		1	W
I_{OUT}	DC Output Current		±20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–1 –5	1 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com. Ind.	–1 –5	1 5	µA

Notes:
1. V_{IL} (min.) = –0.3V (DC); V_{IL} (min.) = –2.0V (pulse width ≤ 2.0 ns).
   V_{IH} (max.) = V_{CC} + 0.3V (DC); V_{IH} (max.) = Vcc + 2.0V (pulse width ≤ 2.0 ns).
2. The Vcc operating range for 8 ns is 3.3V +10%, -5%.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-8 ns		-10 ns		-12 ns		-15 ns		
Sym.	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	170 180	— —	150 160	— —	140 150	— —	130 140	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	30 40	— —	30 40	— —	30 40	— —	30 40	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≤ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— —	10 15	— —	10 15	— —	10 15	— —	10 15	mA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	3	—	4	—	5	—	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	3	0	4	0	5	0	6	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3	0	4	0	5	0	6	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

Notes:
1. The Vcc operating range for 8 ns is 3.3V +10%, -5%.

AC TEST LOADS

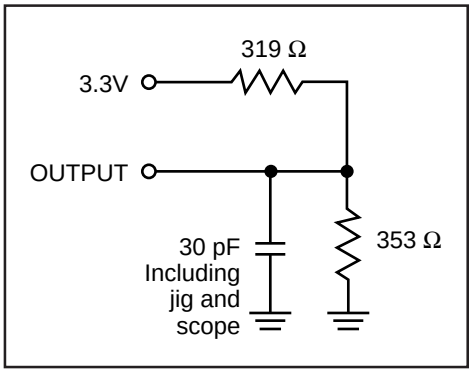


Figure 1.

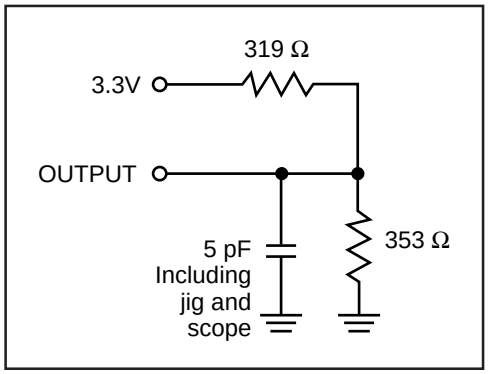
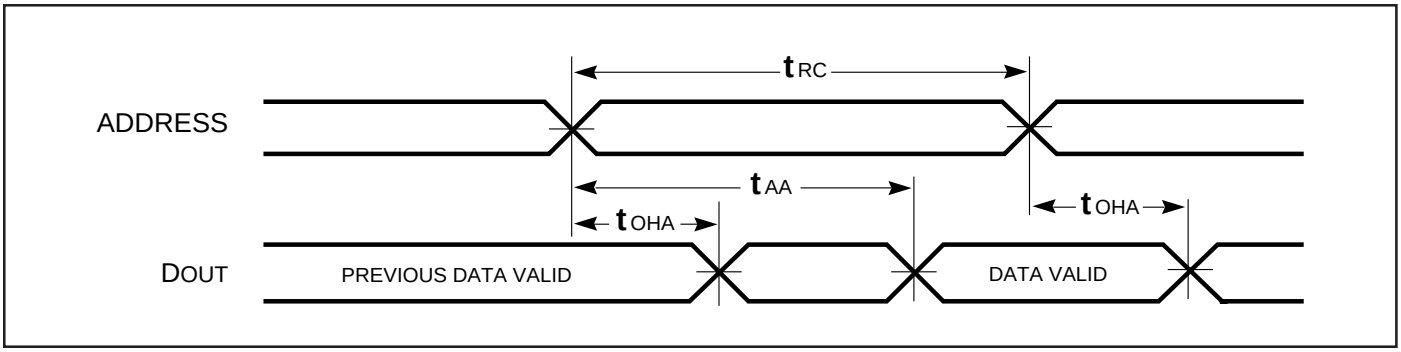


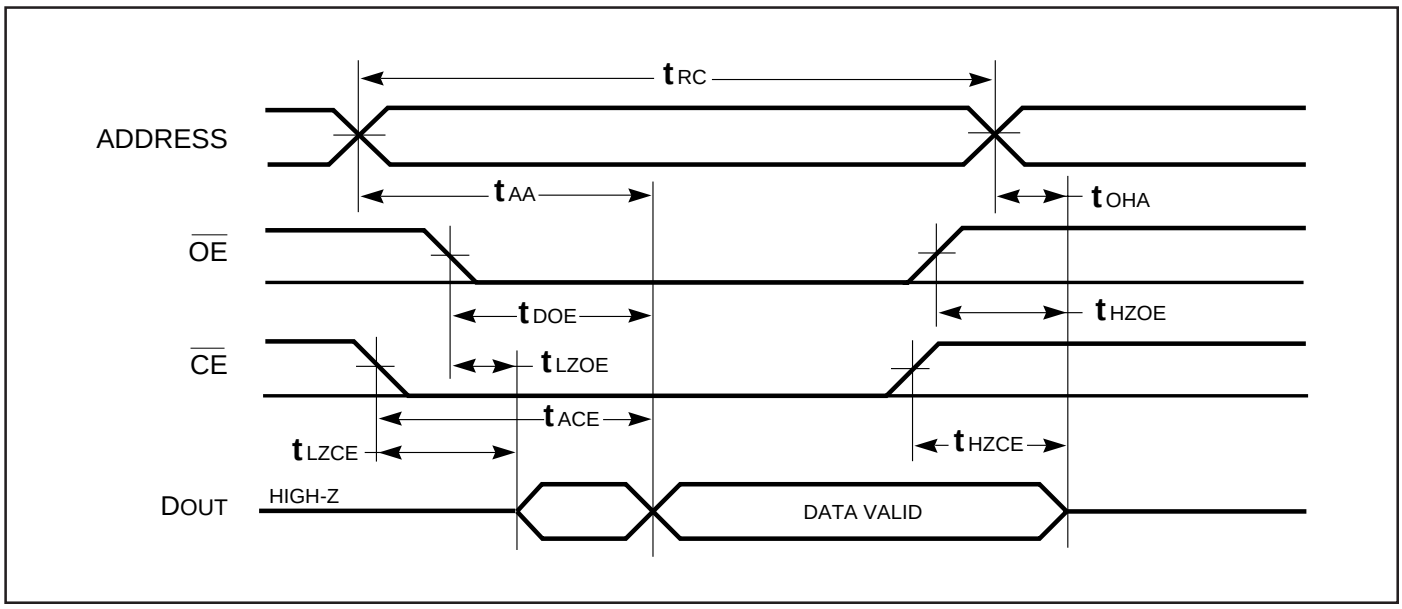
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

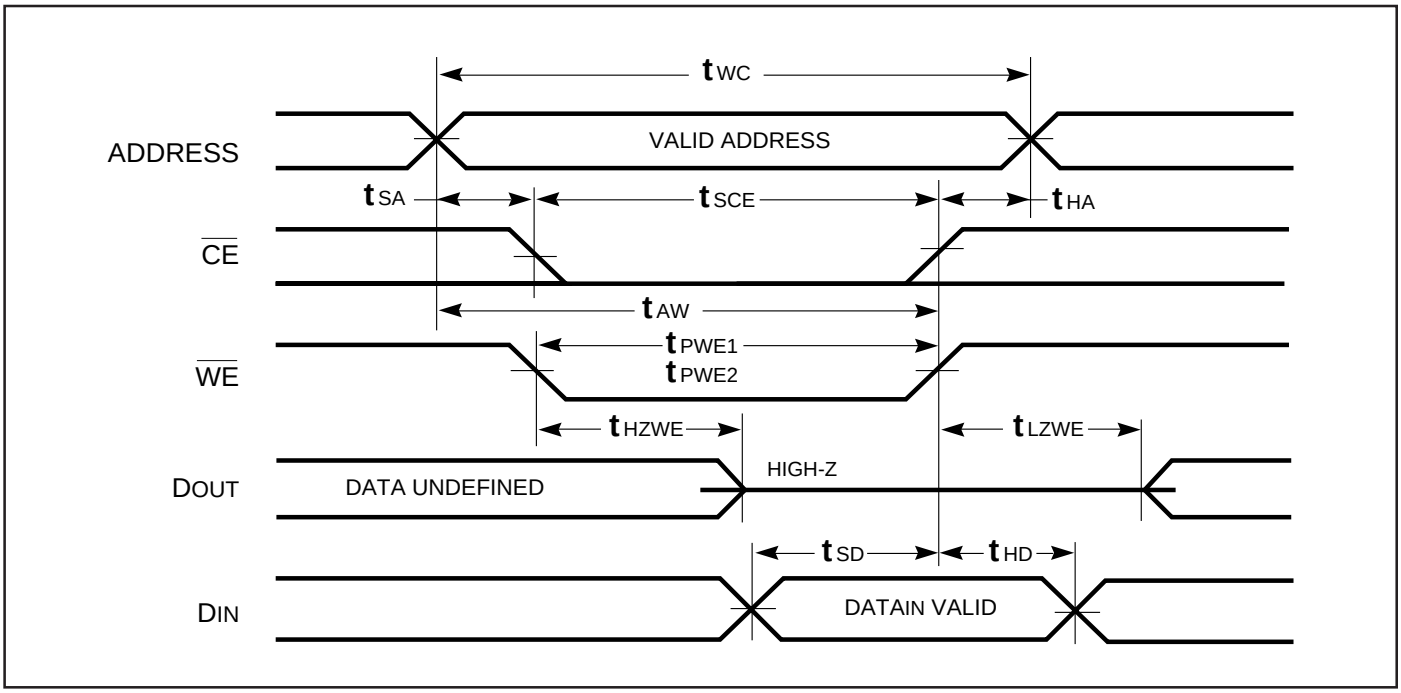
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	8	—	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	7	—	8	—	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	7	—	8	—	9	—	10	—	ns
t_{SD}	Data Setup to Write End	4.5	—	5	—	6	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	3	—	4	—	5	—	6	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

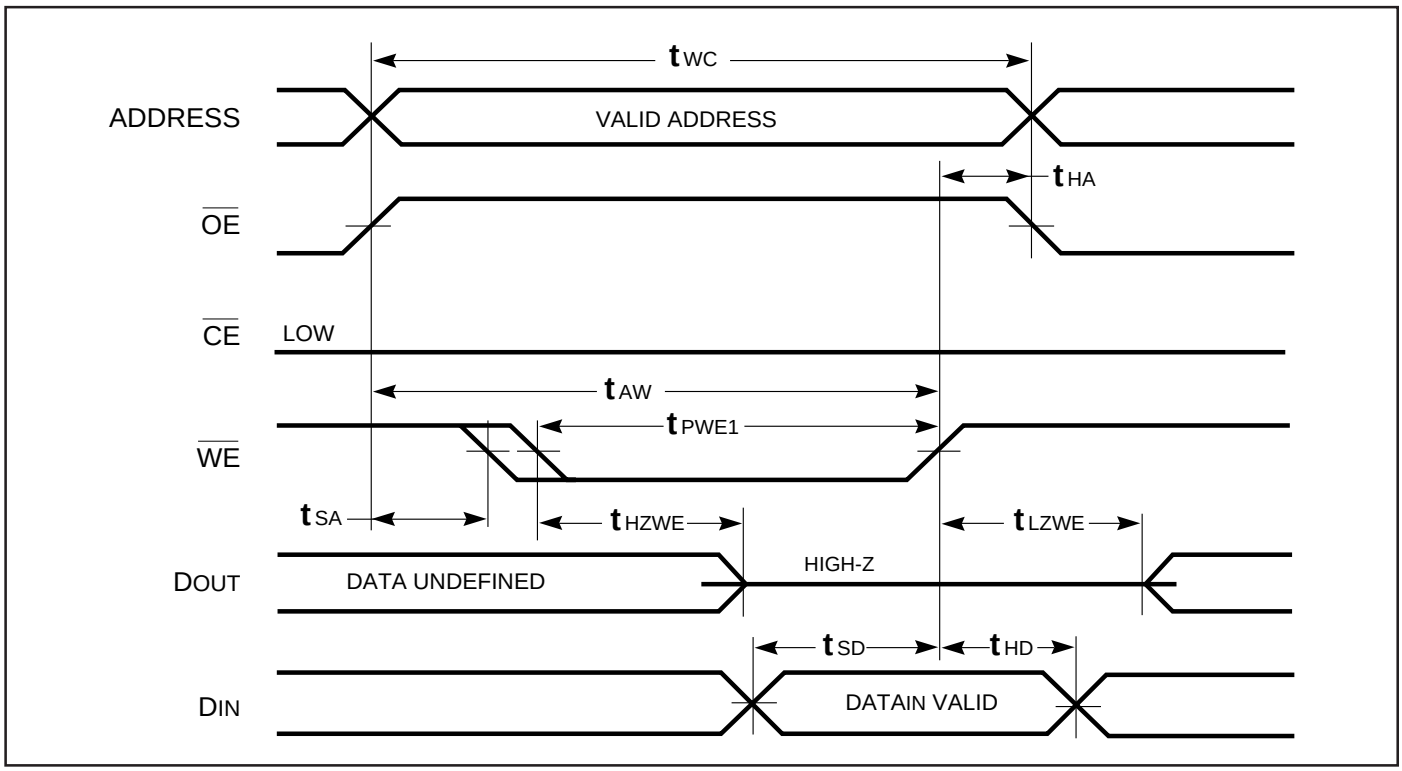
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. Tested with $\overline{OE}$ Hith.

AC WAVEFORMS

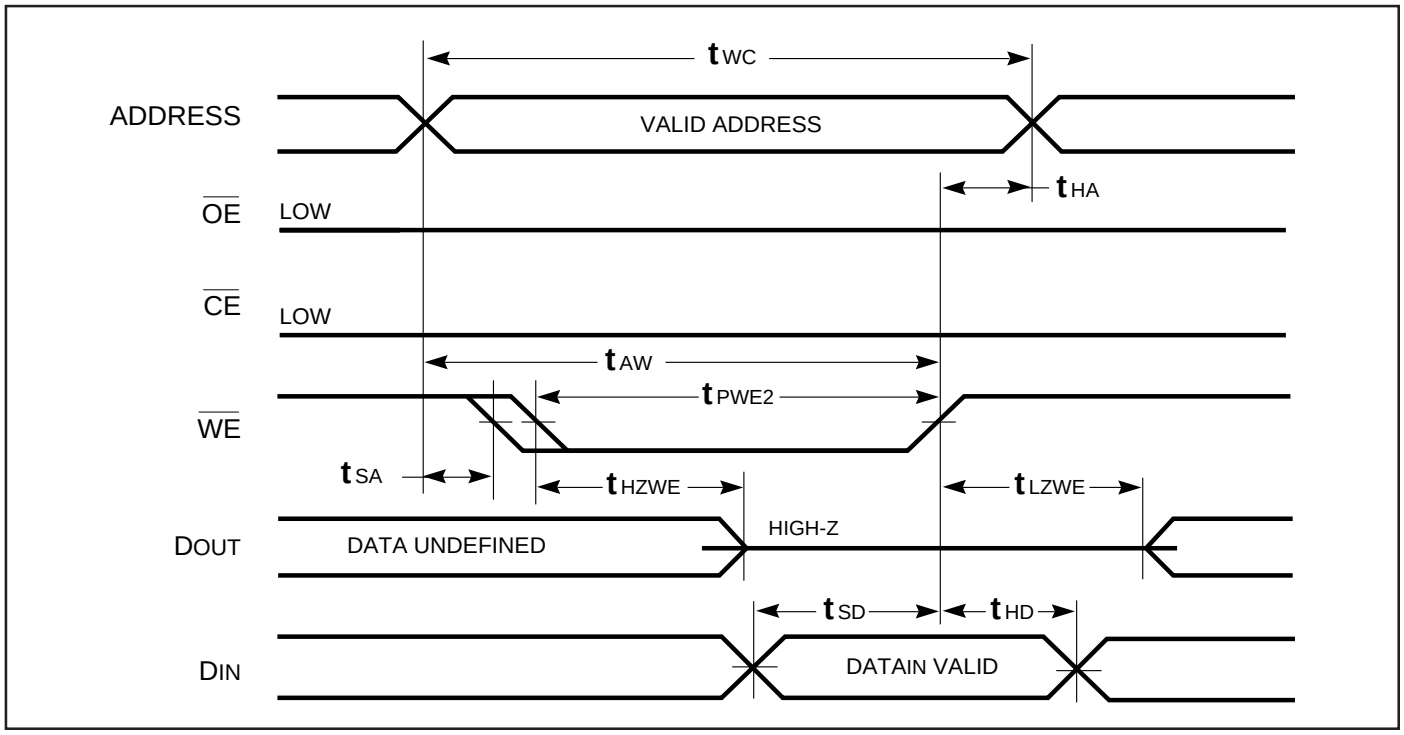
WRITE CYCLE NO. 1 [1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW)



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ is HIGH During Write Cycle) (1,2)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ is LOW During Write Cycle) (1)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed(ns)	OrderPartNo.	Package
8	IC61LV2568-8T	400mil T SOP-2
	IC61LV2568-8K	400mil SOJ
10	IC61LV2568-10T	400mil T SOP-2
	IC61LV2568-10K	400mil SOJ
12	IC61LV2568-12T	400mil T SOP-2
	IC61LV2568-12K	400mil SOJ
15	IC61LV2568-15T	400mil T SOP-2
	IC61LV2568-15K	400mil SOJ

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed(ns)	OrderPartNo.	Package
8	IC61LV2568-8TI	400mil T SOP-2
	IC61LV2568-8KI	400mil SOJ
10	IC61LV2568-10TI	400mil T SOP-2
	IC61LV2568-10KI	400mil SOJ
12	IC61LV2568-12TI	400mil T SOP-2
	IC61LV2568-12KI	400mil SOJ
15	IC61LV2568-15TI	400mil T SOP-2
	IC61LV2568-15KI	400mil SOJ

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